WHAT IS CLAIMED IS:

1. A semiconductor memory device having a cell-transistor structure in which a word-line of an adjacent cell and a word-line of an own cell are formed adjacent to each other, comprises an n-type diffusion layer having an n-type carrier concentration higher at the region close to the word-line of the own cell than at the region close to the word-line of the adjacent cell.

2. A semiconductor memory device having a cell-transistor structure in which a word-line of an adjacent cell and a word-line of an own cell are formed adjacent to each other, comprises an n-type diffusion layer having a n-type impurity concentration obtained by phosphorus or arsenic higher at the region close to the word-line of the own cell than at the region close to the word-line of the adjacent cell.

3. A semiconductor memory device having a cell-transistor structure in which a word-line of an adjacent cell and a word-line of an own cell are formed adjacent to each other, comprises an n-type diffusion layer having a n-type impurity concentration obtained by boron lower at the region close to the word-line of the own cell than at the region close to the word-line of the adjacent cell.

4. A semiconductor memory device having a cell-transistor structure comprising a side-wall channel of an STI (Shallow Trench Isolation) trench with high concentration of boron.

5. A method for manufacturing a semiconductor memory device having a cell-transistor structure, comprising a step of,

preceding to the step of gate oxidation,

carrying out, in an n-type diffusion layer formed of a word line of an adjacent cell and a word line of an own cell, an ion-implantation for implanting phosphorus or arsenic into an active region close to an adjacent word-line of an adjacent cell by the use of a mask.

6. A method for manufacturing a semiconductor memory device having a cell-transistor structure, comprising the steps of:

directly after forming a shallow trench by STI (Shallow Trench Isolation) using an SiN mask;

ion-implanting phosphorus or arsenic from the point parallel to the longitudinal direction of the active region except for the STI region toward an STI side-wall with taking an oblique line, and

removing an ion-implanted region of the bottom portion of the STI shallow trench.

7. A method for manufacturing a semiconductor memory device having a cell-transistor structure, comprising a step of:

directly after forming a shallow trench by STI (Shallow Trench Isolation) using an SiN mask;

ion-implanting, with a rotation at a predetermined angle, phosphorus or arsenic from the point parallel to the longitudinal direction of the active region except for the STI region toward an STI side-wall with taking an oblique line.

8. A method for manufacturing a semiconductor memory device having a cell-transistor structure, comprising a step of,

preceding to the step of gate oxidation,

carrying out, in an n-type diffusion layer formed of a word line of an adjacent cell and a word line of an own cell, an ion-implantation for implanting phosphorus into an active region except for the region close to an adjacent word-line of an adjacent cell by the use of a mask.

9. A method for manufacturing a semiconductor memory device having a cell-transistor structure, comprising a step of:

directly after forming a shallow trench by STI (Shallow Trench Isolation) using an SiN mask;

ion-implanting phosphorus from the point parallel to the longitudinal

direction of the active region except for the STI region toward an STI side-wall with taking an oblique line.